Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (canceled)

11. (currently amended) An electronic memory component, comprising:

a receiving substrate, wherein the receiving substrate is doped;

a memory cell matrix embedded in the receiving substrate;

a top/protective substrate to at least partially surround the receiving substrate on at least one side of the receiving substrate remote from the memory cell matrix, wherein the top/protective substrate is doped opposite to the receiving substrate; and

a circuit arrangement in contact with at least one substrate of the receiving substrate and the top/protective substrate for detection of a voltage or a current from the at least one substrate of the receiving substrate and the top/protective substrate, other than from a dedicated light sensor circuit component, in response to generation of charge carriers in the at least one substrate upon light incidence on the electronic memory component.

12. (previously presented) The electronic memory component of claim 11, wherein the circuit arrangement comprises a comparator circuit.

13. (previously presented) The electronic memory component of claim 12, wherein the comparator circuit is connected with the receiving substrate, via an electrical contact, to detect the voltage or the current in the receiving substrate.

14. (previously presented) The electronic memory component of claim 12, wherein the comparator circuit is connected with the top/protective substrate, via an electrical contact, to detect the voltage or the current in the top/protective substrate.

15. (previously presented) The electronic memory component of claim 11, wherein the electronic memory component is configured to deny access to the memory component in response to detection by the circuit arrangement of the voltage in excess of a limit voltage or the current in excess of a limit current.

16. (previously presented) The electronic memory component of claim 11, wherein the electronic memory component is configured to emit an alarm to a controlling central processing unit (CPU) in response to detection by the circuit arrangement of the voltage in excess of a limit voltage or the current in excess of a limit current.

17. (previously presented) The electronic memory component of claim 11, wherein the top/protective substrate comprises a well to surround the receiving substrate.

18. (previously presented) The electronic memory component of claim 11, further comprising a carrier substrate, wherein the top/protective substrate is associated with the carrier substrate.

19. (previously presented) The electronic memory component of claim 18, wherein the top/protective substrate is buried in the carrier substrate.

20. (previously presented) The electronic memory component of claim 18, wherein:
the receiving substrate comprises a p-doped substrate;
the top/protective substrate comprises an n-doped substrate; and
the carrier substrate comprises another p-doped substrate.

21. (previously presented) The electronic memory component of claim 11, further comprising:
an external source associated with the memory cell matrix, wherein the external source comprises a contact;
a bitline associated with the memory cell matrix;
a wordline associated with the memory cell matrix; and
a control gate associated with the memory cell matrix.

22. (previously presented) The electronic memory component of claim 11, wherein the electronic memory component comprises an erasable programmable read only memory (EPROM), an electrical erasable programmable read only memory (EEPROM), or a Flash memory.

23. (previously presented) The electronic memory component of claim 11, wherein the electronic memory component is configured to continuously detect for light incidence in the form of a light attack.

24. (previously presented) The electronic memory component of claim 11, wherein the electronic memory component is on a smart card.

25. (new) The electronic memory component of claim 13, wherein the receiving substrate comprises an integral, large-area light sensor to generate the charge carriers in the receiving substrate, wherein the receiving substrate is configured to generate the charge carriers in response to the light incidence on any part of the receiving substrate.

26. (new) The electronic memory component of claim 13, wherein the receiving substrate covers a majority of a surface area of the electronic memory component, wherein the receiving substrate is configured to generate the charge carriers in response to the light incidence on any part of the receiving substrate.

27. (new) The electronic memory component of claim 14, wherein the top/protective substrate comprises an integral, large-area light sensor to generate the charge carriers in the top/protective substrate, wherein the top/protective substrate is configured to generate the charge carriers in response to the light incidence on any part of the top/protective substrate.

28. (new) The electronic memory component of claim 14, wherein the top/protective substrate covers a majority of an area of the electronic memory component, wherein the top/protective substrate is configured to generate the charge carriers in response to the light incidence on any part of the top/protective substrate.